REMARKS

This Amendment is in response to the Office Action mailed April 30, 2002, which sets a three-month period for response. Reconsideration and withdrawal of the rejections of this application are respectfully requested in view of this amendment and remarks herewith.

Amended claims 1-6 and new claims 23-33 are now pending in this application.

Applicants disagree with the rejections made in the April 30, 2002 Office Action, however, in the interest of expediting prosecution of this patent application, claims 1-6 are amended, claims 7-22 are canceled and new claims 23-33 are added.

Support for the amended recitation in claims 1-6 and new claims 23-33 can be found in the originally filed specification. Specifically, amendment to claim 3 can be found on page 18, lines 5 to 14; amendment to claim 5 can be found on page 29, lines 4 to 16; newly presented claims 23 to 33 can be found on page 27, line 27 to page 28, line 7; Figure 5E, page 17, line 7 to page 21, line 24, page 26, line 3 to page 29, line 3 and throughout the application. Applicants reserve the right to pursue canceled subject matter in a continuation application.

No new matter is added.

It is submitted that these claims, as originally presented, are patentably distinct over the references cited by the Examiner, and that these claims were in full compliance with the requirements of 35 U.S.C. §112. Changes to these claims and the addition of the new claims, as presented herein, are not made for the purpose of patentability within the meaning of 35 U.S.C. §§101, 102, 103 or 112. Rather, these

changes and additions are made simply for clarification and to round out the scope of protection to which Applicants are entitled.

Applicants re-affirm their election of claims 1 to 6 for further prosecution of this application. Claims 7-22 are withdrawn from consideration pursuant to 37 C.F.R. § 1.142(b), as being drawn to nonelected subject matter.

Applicants cancel claims 7-22 without prejudice. Applicants, however, reserve the right to rejoin any and all canceled subject matter without prejudice, admission, surrender or any intention to create any estoppel as to equivalents. Applicants also reserve the right to pursue canceled subject matter in a continuation application.

Claims 3 and 5 are rejected to under 35 U.S.C. §112, second paragraph as said to be indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Applicants respectfully submit that amended claims 3 and 5 as presented herein are not indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Accordingly, it is respectfully requested that the 112 rejections of claims 3 and 5 be withdrawn.

Claims 1 to 5 are rejected under 35 U.S.C. § 102(b) as said to be anticipated by Imaoka et al., U.S. Patent No. 5,426,073 ("Imaoka"). Claim 6 is rejected under 35 U.S.C. §103(a) as said to be unpatentable over Imaoka in view of Chou U.S. Patent No. 5,578,516 ("Chou"). Applicants submit that the independent claims (claims 1 and 6) as amended are patentable over Imaoka and Chou. Applicants therefore respectfully traverse the rejections.

The present invention claims and discloses a method of manufacturing a semiconductor device having uneven portions such as a trench capacitor and a damascene wiring, in which the particle generation causing the manufacturing yield of the semiconductor device to be lowered is suppressed by grinding or polishing the peripheral portion and beveled portion on the main surface of a target substrate such as a semiconductor substrate, and the contamination of the semiconductor substrate and the processing machine by the filled metal in metallization trench such as a copper trench is suppressed. According to the present invention, the method is performed by "selectively grinding or polishing the peripheral portion and the beveled portion on the main surface side of a target substrate including a semiconductor substrate so as to keep a diameter of the semiconductor substrate substantially unchanged."

For example, claim 1 recites,

> "A method of manufacturing a semiconductor device in which a semiconductor element is formed in a semiconductor substrate, including selectively grinding or polishing the peripheral portion and the beveled portion on the main surface side of a target substrate including a semiconductor substrate **so as to keep a diameter of said semiconductor substrate substantially unchanged**."
>
> (Emphasis added).

Claim 6 contains similar limitations.

These features are supported by the following descriptions:

(i) As shown in FIGS. 3-5, the peripheral portion and beveled portion on the main surface side of a silicon wafer are polished so as to keep the diameter unchanged;

(ii) The grinding or polishing device of a silicon wafer shown in FIG. 6 and a third embodiment has "a polishing plate 103 capable of fixation at an optimum polishing angle relative to the peripheral portion on the side of the main surface of the target substrate 100"; and

(iii) Since the grinding or polishing is performed so as to keep the diameter of a silicon wafer substantially unchanged as described in the specification, from page 32, line 16 to page 33, line 1, the step of grinding or polishing can be introduced freely into the manufacturing process without bringing about any inconvenience in the wafer transfer system of the manufacturing apparatus.

With respect to claim 1, the Office Action asserted that Imaoka "discloses the claimed method of manufacturing a semiconductor device in which a semiconductor element is formed in a semiconductor substrate including a step of selectively grinding or polishing the peripheral portion and the beveled portion on the side of the main surface of a target substrate including a semiconductor substrate to remove contamination formed from deposited films in making the semiconductor device..." (Office Action at 4).

The grinding device, however, cited in Imaoka, (*See* Imaoka, column 5, line 21) is used for grinding the peripheral edge of a silicon wafer along the side surface perpendicular to the wafer surface.

More specifically, Imaoka's grinding device in Japanese Unexamined Patent Publication Tokukai Sho 62-154614 ("Imaoka '614"), stacked wafers 18 are pressed by shafts 32a and 32b coaxially arranged. When the shafts 32a and 32b are

axially rotated in the direction shown by an arrow 32c, the stacked wafers 18 move back and forth in the horizontal direction shown by an allow 32d. While moving the shafts in this way, a disk-form grind wheel 33 is rotated axially as shown by an arrow 33c, with the result that the peripheral edge of the cylinder formed of the stacked wafers 18 is ground up to 101 mm. After individual stacked wafers are separated from the stacked wafers 18, the separated wafers are subjected to a chamfering process to obtain wafers of 100 mm diameter (*See* Imaoka '614, FIG. 3; and page 3, upper right column to lower left column).

Additionally, FIG. 3B of Imaoka shows that the peripheral edge is ground so as to reduce the width of the wafer edge by GW (Grinding width) = 0.5 to 20 mm (*See* Imaoka, FIG. 3B; and column 5, lines 21-24). Similarly, Imaoka describes the periphery of the wafer is ground so as to reduce the diameter of a wafer as shown in Figs. 4 and 5. Also, in Imaoka the periphery of a 6-inch wafer is ground to obtain a 4 or 5 inch wafer (*See* Imaoka column 7, lines 11-18).

That is, the method of grinding or polishing a silicon substrate disclosed in Imaoka includes the step of grinding the entire periphery of an underlying silicon wafer 1 by a grinding wheel to reduce the wafer edge by GW = 0.5 to 20 mm. In this manner, a multiple layer 2 including a protrusion 2' is removed. In addition, the wafer edge thus ground is rounded by a chamfering process to completely remove the protrusion 2', thereby providing mirror finish (*See* Imaoka FIG. 3B; and column 5, lines 1 to 28).

In contrast, in the method of grinding or polishing a silicon substrate according to the present invention, an uneven portion produced by anisotropic dry etching treatment in the peripheral position 1a and the beveled portion 1b of a main surface side of a substrate is removed (through grinding or polishing) "so as to keep a diameter of the

semiconductor substrate substantially unchanged" (e.g., *See* specification, FIGS. 3F and 4B).

Additionally, in the grinding or polishing step for a silicon substrate according to the present invention, a film formed of a metal material having a strong contamination effect such as copper and covering the peripheral portion 1a and beveled portion 1b of the main surface side of a substrate is removed by grinding or polishing "so as to keep a diameter of the semiconductor substrate substantially unchanged."

The difference between the present invention and Imaoka is supported by difference in structure between the device of Imaoka, for grinding the wafer edge along the side surface perpendicular to a wafer surface and the device of the present invention for grinding or polishing the wafer surface shown in FIG. 6 having a polishing plate, the polishing angle of which can be optimized.

With respect to claim 6, the Office Action admits that it does not expressly teach forming the uneven portion by applying an anisotropic dry etching treatment but the anisotropic dry etching treatment is a well-known technique for forming the uneven portion (*See* Chou).

The uneven portion of the present invention is the one produced by dry etching and differs from the protrusion 2' formed in the multiple layer shown in FIG. 3(a) of Imaoka. Furthermore, the grinding or polishing method of the present invention for removing the uneven portion differs from that of the Imaoka. Consequently, claim 6 cannot be achieved without hindsight reconstruction and improper combination of Imaoka and Chou.

Chou, as asserted by the Office Action "...teaches applying the anisotropically dry etching treatment to form the uneven portion (18, fig. 3, col 4 lines 60-54) in the target substrate including the semiconductor substrate" (Office Action, at 5). Chou, however, does not teach or suggest "selectively grinding or polishing the peripheral portion and the beveled portion on the main surface side of a target substrate including a semiconductor substrate so as to keep a diameter of said semiconductor substrate substantially unchanged."

"For a prior art reference to anticipate in terms of 35 U.S.C. 102(b), every element of the claimed invention must be identically shown in a single reference." Scripps Clinic & Research Foundation v. Genetech, Inc., 18 U.S.P.Q.2d 1001 (Fed. Cir. 1991). Since Imaoka does not disclose or suggest every element of the presently claimed invention, the 35 U.S.C. 102(b) rejection based on Imaoka cannot stand. And Imaoka either individually or in any combination, fails to suggest the claimed invention.

Neither Imaoka nor Chou claim and disclose "selectively grinding or polishing the peripheral portion and the beveled portion on the main surface side of a target substrate including a semiconductor substrate so as to keep a diameter of said semiconductor substrate substantially unchanged", Applicants believe that the amended independent claims (claims 1 and 6) are patentable over Imaoka and Chou - taken either alone or in combination.

Moreover, in an obviousness rejection, the standard established in *In re Fritch*, 23 U.S.P.Q.2d 1780, 1783-84 (Fed. Cir. 1992), must be followed. *Fritch* in pertinent part states (with emphasis added):

> Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination. Under Section 103, teachings of references can be combined only if there is some suggestion or incentive to do so . . . . **The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification.**

Even though a reference can be modified in a way that the Examiner suggests, this does not mean that the reference renders the instant invention obvious unless the motivation to do the modification is in the references teaching. It is respectfully submitted that no such teaching exists in the references cited by the current Office Action either alone or in any combination. There is nothing in the reference teachings suggesting the modification or the desirability of the modification. There is no evidence in the Office Action showing why the skilled artisan would have combined the cited references and then would have arrived at the present invention.

There must be some teaching, suggestion, or incentive in the references (and not Applicants' disclosure) that supports the combination of the references. *In re Fine*, 5 U.S.P.Q. 2d 1596, 1599-1600 (Fed. Cir. 1988). No such teaching, suggestion or incentive is in the cited documents.

According to the Board of Patent Appeals and Interferences in the case of *Ex parte Obukowicz*, 27 U.S.P.Q.2d 1063, 1065 (B.P.A.I. 1992) (with emphasis added):

> In proceedings before the Patent and Trademark Office, the Examiner bear the burden of establishing a *prima facie* case of obviousness based upon the prior art. *In re Piasecki*, 745 F.2d 1468, 1471-72, 223 U.S.P.Q. 785, 787-88 (Fed. Cir. 1984). **The Examiner can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally**

> **available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references.** *In re Fine*, 837 F.2d 1071, 1074, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988). **Indeed, the teachings of references can be combined only if there is some suggestion or incentive to do so.** *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 723 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984).

The picking and choosing from both of the cited references to allege that the instant invention is obvious simply fails in light of the case law under Section 103. The Examiner is respectfully invited to cite references for the desirability of modification and the teaching, suggestion or incentive for combination and for modification of the reference teachings or provide an affidavit, as called for by 37 C.F.R. §1.106(b) and M.P.E.P. §706.02(a). Otherwise, it is respectfully submitted that the Section 103 rejection must be withdrawn.

Accordingly, none of cited references, alone, or in any combination, render Applicants' invention *prima facie* obvious. Moreover, none of the references teach or suggest the surprising properties of the presently claimed invention, as shown in the application, which properties, Applicants submit are additionally demonstrative of the patentability of the instant invention.

Consequently, the present invention is not obvious in view of Imaoka and/or Chou, and neither Imaoka nor Chou supply the deficiencies that are claimed and disclosed in the present invention.

Reconsideration and withdrawal of the art rejections under 35 U.S.C. §§ 102(b) and 103(a) are respectfully requested.

Claims 2-5 depend from independent claim 1 and are allowable due to such dependency. Applicants therefore respectfully request that the rejection of claims 2-5 under 35 U.S.C. 102(b) be withdrawn.

Applicants request that due to the above arguments the newly submitted claims (claims 23-33) are also patentable over Imaoka and Chou – taken either alone or in combination.

In view of these amendments and remarks, Applicants respectfully submit that all of the claims (claims 1-6 and 23-33) now pending in the application are in condition for allowance. Applicants respectfully request an early, favorable and expedited reconsideration and prompt issuance of a Notice of Allowance are earnestly solicited.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached pages are captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE".

If any issues remain, or if the Examiner has any further suggestions, the Examiner is invited to call the undersigned at the telephone number provided below.

The Examiner is hereby authorized to charge any insufficient fees or credit any overpayment associated with the above-identified application to Deposit Account No.50-0320.

The Examiner's consideration of this matter is gratefully acknowledged.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Amended) A method of manufacturing a semiconductor device in which a semiconductor element is formed in a semiconductor substrate, including [a step of] selectively grinding or polishing the peripheral portion and the beveled portion on [the side of] the main surface side of a target substrate including a semiconductor substrate to keep a diameter of said semiconductor substrate substantially unchanged.

2. (Amended) The method of manufacturing a semiconductor device according to claim 1, wherein [the step of] selectively grinding or polishing the peripheral portion and the beveled portion on [the side of] the main surface side of the target substrate is carried out after [a step of] forming [an] a deep and irregular uneven portion in the peripheral portion and the beveled portion of the target substrate.

3. (Amended) The method of manufacturing a semiconductor device according to claim 1, wherein [the step of] selectively grinding or polishing the peripheral portion and the beveled portion on [the side of] the main surface side of the target substrate is carried out after at least one additional step, which is included in the manufacturing steps of the semiconductor device, following [a step of] forming [an] a deep and irregular uneven portion in the target substrate.

4. (Amended) The method of manufacturing a semiconductor device according to claim 1, wherein [the step of] selectively grinding or polishing the peripheral portion and the beveled portion on [the side of] the main surface side of the target substrate is carried out after [a step of] covering the main surface of the target substrate with a resist film, said step being carried out [after the step of] following forming [an] a deep and irregular uneven portion in the target substrate.

5. (Amended) The method of manufacturing a semiconductor device according to claim 1, wherein [the step of] selectively grinding or polishing the peripheral portion and the beveled portion on [the side of] the main surface side of the target substrate is carried out after [a step of] forming a film of a material providing a source of contamination of [the] a processing machine for applying a predetermined processing step, which is included in processing steps of the semiconductor device, to the target substrate including the semiconductor substrate or providing a source of contamination of the semiconductor substrate.

6. (Amended) A method of manufacturing a semiconductor device comprising:

applying anisotropic dry etching treatment to form an uneven portion in a target substrate including a semiconductor substrate; and

selectively grinding or polishing the peripheral portion and the beveled portion on [the side of] the main surface side of the target substrate including the semiconductor substrate to keep a diameter of said semiconductor substrate substantially unchanged.